In the Claims:

1. (Currently amended) A module comprising a functional block and a test controller for controlling the functional block in an evaluation mode of the module, the test controller comprising:

a plurality of pins including an input pin and an output pin;

a first register coupled between the input pin and the output pin for receiving a bit pattern via the input pin and outputting the bit pattern via the output pin; and

a second register coupled to the first register for capturing the bit pattern responsive to an update signal;

~~characterized in that the test controller further comprises~~ dedicated control circuitry for blocking the update signal responsive to the bit pattern[[.]];

a multiplexer; and

a no-update bypass register configured with the multiplexer in response to a no-update code, to maintain the bit pattern in a stable state for the evaluation mode.

2. (Original) A module as claimed in claim 1, characterized in that the dedicated control circuitry comprises a first logic gate having:

a first input for receiving the update signal;

a second input coupled to the first register for receiving the bit pattern; and

an output coupled to the second register.

3. (Original) A module as claimed in claim 2, characterized in that the dedicated control circuitry further comprises a plurality of logic gates coupled between the first register and the second input of the first logic gate for providing the second input with the bit pattern in a modified form.

4. (Currently amended) ~~A module as claimed in claim 3, characterized in that the test controller further comprises:~~) A module comprising a functional block and a test controller for controlling the functional block in an evaluation mode of the module, the test controller comprising:

a plurality of pins including an input pin and an output pin;

a first register coupled between the input pin and the output pin for receiving a bit pattern via the input pin and outputting the bit pattern via the output pin; and

a second register coupled to the first register for capturing the bit pattern responsive to an update signal;

dedicated control circuitry for blocking the update signal responsive to the bit pattern;

a first logic circuit for receiving the update signal and

for receiving the bit pattern and being coupled to the second register;

a multiplexer having a control terminal, a first input, a second input, and an output coupled to the output pin;

a third register coupled between the input pin and the first input of the multiplexer; and

a no-update bypass register coupled between the input pin and the second input of the multiplexer;

the control terminal of the multiplexer being responsive to at least a part of the bit pattern.

5. (Original) A module as claimed in claim 4, characterized in that the dedicated control circuitry comprises a second logic gate having:

a first input coupled to the plurality of logic gates for receiving the bit pattern in the modified form;

a second input for receiving a further update signal; and

an output coupled to the third register, the third register being responsive to the further update signal.

6. (Previously presented) A module as claimed in claim 4, characterized in that an output path of the plurality of logic gates comprises a data storage element responsive to the update signal for storing the bit pattern in the modified form.

7. (Currently amended) ~~A module as claimed in claim 2, characterized in that the test controller further comprises:~~ A module comprising a functional block and a test

controller for controlling the functional block in an evaluation mode of the module, the test controller comprising:

a plurality of pins including an input pin and an output pin;

a first register coupled between the input pin and the output pin for receiving a bit pattern via the input pin and outputting the bit pattern via the output pin; and

a second register coupled to the first register for capturing the bit pattern responsive to an update signal;

dedicated control circuitry for blocking the update signal responsive to the bit pattern;

a first logic circuit for receiving the update signal;

for receiving the bit pattern; and

coupled to the second register;

a ~~further~~ multiplexer having a first input, a second input, an output and a control terminal coupled to an output of the second register;

a first further register coupled between the input pin and the first input of the further multiplexer;

a second further register being responsive to the update signal, the second further register having at least an input coupled to the first further register; and a conductor coupled between the input pin and the second input of the further multiplexer;

the first register being coupled between the output of the multiplexer and the output pin; and

the second input of the first logic gate being coupled to the first register via the second register.

8. (Original) A module as claimed in claim 7, characterized in that the second further register is responsive to a reset signal.

9. (Previously presented) A module as claimed in claim 7, characterized in that the second input of the first logic gate is coupled to the second register through a further logic gate, the further logic gate further being coupled to the first register.

10. (Previously presented) A module as claimed in claim 7, characterized in that the dedicated control circuitry further comprises a plurality of logic gates being responsive to the bit pattern in the second register, the plurality of logic gates having their inputs coupled to the second further register and having at least an output coupled to the control terminal of the further multiplexer.

11. (Currently amended) An electronic device comprising a plurality of modules being substantially serially interconnected in an evaluation mode through respective input pins and output pins, a module from the plurality of interconnected modules comprising a functional block and a test controller for controlling the functional block in the evaluation mode of the module, the test controller comprising:

a plurality of pins including an input pin from the respective input pins and an output pin from the respective output pins;

a first register coupled between the input pin and the output pin for receiving a bit pattern via the input pin and outputting the bit pattern via the output pin; and a second register coupled to the first register for capturing the bit pattern responsive to an update signal;

a by-pass register and a multiplexer for directing data to the output pin;

~~characterized in that the test controller further comprises~~ dedicated control circuitry for blocking the update signal responsive to the bit pattern and providing data-path stability for the evaluation mode.

12. (Original) An evaluation tool comprising a set of bit patterns for evaluating an electronic device as claimed in claim 11 by providing the electronic device with the set of bit patterns, characterized in that the set of bit patterns comprises a bit pattern for triggering the control circuitry to block the update signal responsive to the bit pattern.

13. (Previously presented) A test controller circuit for controlling a functional block in an evaluation mode, the test controller comprising:

a plurality of pins including an input pin and an output pin;

a multiplexer having a first input, a second input, an output coupled to the output pin, and a control terminal responsive to at least a part of the bit pattern;

a no-update bypass register coupled between the input pin and the second input of the multiplexer;

a first register, coupled between the input pin and the output pin, to receive a bit pattern via the input pin and to output the bit pattern via the output pin; and

a second register, coupled to the first register, to capture the bit pattern responsive to an update signal;

a third register coupled between the input pin and the first input of the multiplexer; and

dedicated control circuitry to block the update signal responsive to the bit pattern, the control circuitry including

a first logic gate having a first input for receiving the update signal, a second input coupled to the first register for receiving the bit pattern, and an output coupled to the second register, and

a plurality of logic gates coupled between the first register and the second input of the first logic gate for providing the second input with the bit pattern in a modified form.

14. (Previously presented) The circuit of claim 13, wherein the dedicated control circuitry includes a second logic gate having

a first input coupled to the plurality of logic gates for receiving the bit pattern in the modified form,

a second input for receiving a further update signal, and

an output coupled to the third register, the third register being responsive to the further update signal.

15. (Previously presented) The circuit of claim 14, further including a data storage element that is coupled to an output of the plurality of logic gates and that is responsive to the update signal for storing the bit pattern in the modified form.

16. (Previously presented) The circuit of claim 13, further including a data storage element that is coupled to an output of the plurality of logic gates and that is responsive to the update signal for storing the bit pattern in the modified form.